What is claimed is:

1. A memory device with vertical transistors and trench capacitors, comprising:

a substrate, having at least one deep trench therein;

a trench capacitor, deposited in a lower position of the deep trench;

a conducting structure, deposited on the trench capacitor, comprising a first conductive layer and a second conductive layer;

a ring shaped insulator, deposited on parts of the sidewall of the deep trench and between the substrate of the deep trench and the first conductive layer, such that the first conductive is surrounded by the ring shaped insulator, wherein the second conductive layer is deposited on the first conductive and the ring shaped insulator;

a diffusion barrier, deposited on one side of the sidewall of the deep trench and between the second conductive layer and the substrate of the deep trench;

a trench top isolation, deposited on the conducting structure; and

a control gate, deposited on the trench top isolation.

2. The memory device as claimed in claim 1, further comprising:

a buried strap, deposited within the substrate beside parts of the conducting structure where the diffusion barrier is not deposited, serving as a source.

3. The memory device as claimed in claim 1, further comprising:

a doping area, provided within the substrate beside the control gate, serving as a drain.

4. The memory device as claimed in claim 1, wherein the ring shaped insulator comprises an oxide.

5. The memory device as claimed in claim 1, wherein the first conductive layer comprises a doped polysilicon or a doped amorphous silicon.

6. The memory device as claimed in claim 1, wherein the second conductive layer comprises a doped polysilicon or a doped amorphous silicon.

7. The memory device as claimed in claim 1, wherein the diffusion barrier comprises an oxide.

8. The memory device as claimed in claim 1, wherein the thickness of the diffusion barrier is substantially less than 100Å.

9. The memory device as claimed in claim 1, wherein the trench top isolation comprises an oxide.

10. The memory device as claimed in claim 1, wherein the control gate comprises a gate layer and a

gate dielectric layer deposited between the gate layer and the substrate.

11. The memory device as claimed in claim 1, wherein the gate layer comprises a polysilicon, a silicide, a metal layer, or a combination thereof.

12. The memory device as claimed in claim 1, wherein the gate dielectric layer comprises an oxide.

13. The memory device as claimed in claim 2, wherein the buried strap is electrically connected with the control gate and formed by diffusing dopants of the first conductive layer into the substrate of the trench surrounding the top of the second conductive layer.

14. A method of fabricating a memory device with vertical transistors and trench capacitors, comprising:

providing a substrate;

forming at least one deep trench in the substrate;

forming a trench capacitor in a lower position of the deep trench;

forming a ring shaped insulator on the sidewall of the deep trench above the trench capacitor, wherein a space is surrounded by the ring shaped insulator ;

forming a first conductive layer to fill the space;

forming a diffusion barrier on one side of the sidewall of the deep trench above the ring shaped insulator;

forming a second conductive layer on the first conductive layer and the ring shaped insulator and beside the diffusion barrier;

forming a trench top isolation on the second conductive layer and the diffusion barrier; and

forming a control gate on the trench top isolation.

15. The method as claimed in claim 14, further comprising:

forming a buried strap within the substrate beside parts of the second conductive layer where the diffusion barrier is not deposited to serve as a source.

16. The method as claimed in claim 14, further comprising:

forming a doping area within the substrate beside the control gate to serve as a drain.

17. The method as claimed in claim 14, wherein the ring shaped insulator comprises an oxide.

18. The method as claimed in claim 14, wherein the first conductive layer comprises a doped polysilicon or a doped amorphous silicon.

19. The method as claimed in claim 14, wherein the second conductive layer comprises a doped polysilicon or doped amorphous silicon.

20. The method as claimed in claim 14, wherein the diffusion barrier comprises an oxide.

21. The method as claimed in claim 14, wherein the thickness of the diffusion barrier is substantially less than 100Å.

22. The memory device as claimed in claim 14, wherein the trench top isolation comprises an oxide.

23. The method as claimed in claim 14, wherein the control gate comprises a gate layer and a gate dielectric layer deposited between the gate layer and the substrate.

24. The method as claimed in claim 14, wherein the gate layer comprises a polysilicon, a silicide, a metal layer, or a combination thereof.

25. The method as claimed in claim 13, wherein the gate dielectric layer comprises an oxide.

26. The method as claimed in claim 15, wherein the buried strap is formed by diffusing the dopants of the first conductive layer into the substrate during annealing so as to electrically connect with the control gate.

27. A method of fabricating a memory device with vertical transistors and trench capacitors, comprising:

providing a substrate;

forming at least one deep trench in the substrate;

forming a trench capacitor in a lower position of the deep trench;

forming a ring shaped insulator on the sidewall of the deep trench above the trench capacitor,

wherein a space is surrounded by the ring shaped insulator ;

forming a first conductive layer to fill the space;

performing a nitridation in the substrate of the bottom and one side of the sidewall of the deep trench;

performing a oxidation in the substrate of the bottom and the sidewall of the deep trench to form a thick oxide layer and a thin oxide layer, wherein the thin oxide layer is formed on parts of the substrate where nitridation has been performed, the thick oxide layer is formed on parts of the substrate without nitridation;

removing the thin oxide layer;

forming a second conductive layer on the first conductive layer and the ring shaped insulator;

etching parts of the thick oxide layer using the second conductive layer as a mask so as to form a diffusion barrier between the second conductive layer and one side of the sidewall of the trench;

forming a trench top isolation on the second conductive layer and the diffusion barrier; and

forming a control gate on the trench top isolation.

28. The method as claimed in claim 27, further comprising:

forming a buried strap within the substrate beside parts of the second conductive layer where the

diffusion barrier is not deposited to serve as a source.

29. The method as claimed in claim 27, further comprising:

forming a doping area within the substrate beside the control gate to serve as a drain.

30. The method as claimed in claim 27, wherein the ring shaped insulator comprises an oxide.

31. The method as claimed in claim 27, wherein the first conductive layer comprises a doped polysilicon or doped amorphous silicon.

32. The method as claimed in claim 27, wherein the second conductive layer comprises a doped polysilicon or doped amorphous silicon.

33. The method as claimed in claim 27, wherein the diffusion barrier comprises an oxide.

34. The method as claimed in claim 27, wherein the thickness of the diffusion barrier is substantially less than 100Å.

35. The method as claimed in claim 27, wherein the trench top isolation comprises an oxide.

36. The method as claimed in claim 27, wherein the control gate comprises a gate layer and a gate dielectric layer deposited between the gate layer and the substrate.

37. The method as claimed in claim 27, wherein the gate layer comprises a polysilicon, a silicide, a metal layer, or the combination thereof.

38. The method as claimed in claim 36, wherein the gate dielectric layer comprises an oxide.

39. The method as claimed in claim 28, wherein the buried strap is formed by diffusing the dopants of the first conductive layer into the substrate during annealing so as to electrically connect with the control gate.

40. The method as claimed in claim 27, wherein the nitridation is performed by nitrogen-containing ion implantation into the substrate according a certain tilting angle.

41. The method as claimed in claim 40, wherein the certain tilting angle is about 5~10°.

42. The method as claimed in claim 27, wherein the oxidation is performed by thermal oxidation.